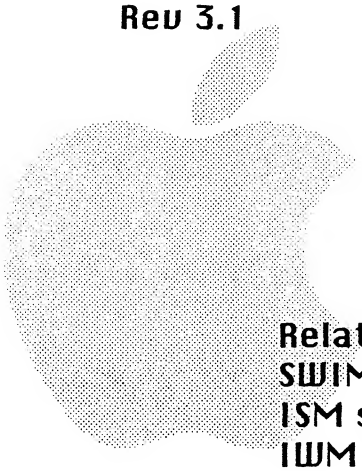
SWIM2 ASIC ERS

Apple Computer

Rev 3.1



Related Documents:
SWIM chip specification
ISM specification
IWM specification
Apple spec 699-0321
Apple spec 699-0477

Rev 2.0 changes

The following changes were made in Rev 2.0.

1. The motor timeout has been removed.
2. A new bit in the setup register to invert the wrdata was added.
3. Dat1byte has changed.
4. Write pulse width spec added.

These changes are shown in italics in the text.

Rev 3.0 changes

The following changes were make in Rev 3.0.

1. Dat1byte is gated with error in write mode.
2. Test mode changed and now has a definition.

These changes are shown in italics in the text.

Rev 3.1 changes

1. Motoron pin definition is modified to reflect the hardware.

These changes are shown in italics in the text.

Introduction

The purpose of SWIM2 is to provide a low cost replacement to the SWIM ASIC with enhanced functionality to extend its usefulness to the next generation of floppy disk drives. It is the intent of the design to offer 800K GCR support in a manner currently being used by the PIC in Zone 5 (an ISM like machine with windows set for GCR cells). MFM format will be supported at two data rates, the current 1.44M byte 500KHz, and a new 2.88M byte 1MHz.

There are many features included in the current SWIM design which are not used by the software drivers or were proven not to be functional after the design was finished. None of these features will be implemented in the SWIM2 design in order to simplify the design effort. These include ISM error correction (sometimes called the digital phase-lock loop) and post compensation modes.

The SWIM2, unlike the SWIM, will consist of only one set of disk control logic. The write machine will be capable of writing GCR 2,4,6 uS cells, or MFM with software selectable fixed cells. The data separator will have GCR and MFM modes with fixed 2,4,6 uS cell times in GCR mode and two sets of software selectable windows in MFM mode (2,3,4 us and 1,1.5,2 us). The bus interface to the CPU will follow the SWIM convention as a programming model.

High speed MFM mode for new products will be supported by supplying a 32 MHz clock as opposed to the 16MHz clock. It will be possible to run the 1 MHz MFM using a 16 MHz clock but the error rate may increase due to the lack of clock resolution. Since it is difficult to be sure at this time, by supporting 32 MHz clock input we can be sure to have adequate timing resolution.

Programming Model

The SWIM2 retains the ISM bus interface but removes all of the sophisticated error correction modes of the ISM. The assumption is that data from the drive will be processed through a phase lock loop so that data separation is a relatively simple task . The flexibility to set cell times and windows, choose GCR or MFM format, and set write pre-comp parameters is all that remains from the ISM. Unless noted the register description is identical to the ISM.

Register Description

$0 Data Read or write data to or from FIFO. If a Mark byte is read from this location an error is set. (note SWIM provided error correction data on a read here with action not set, SWIM2 will read all zeroes with action not set)

$1 Mark Read or write Mark bytes. A write will cause the missing transition to be generated. A read of a Mark byte from this location will not cause an error.

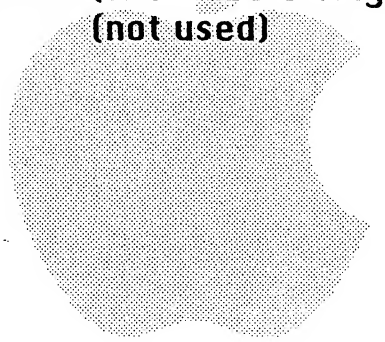
$2 Error Indicates the type of error that has occurred. Cleared on a reset or on read. Only one error can be set at a time. Must be cleared prior to a read or write. If any of these bits are set the error flag in the Handshake register will be set. Errors on reads only function in MFM mode after the mark byte is found.

Data 0	Underrun FIFO. FIFO empty while writing or full and not read during a read.
Data1	Mark in data. Mark byte read from data register
Data 2	Overrun FIFO. FIFO written while full in write mode or read while empty in read mode.
Data 3	Not used (was correction error)
Data 4	Transition too short
Data 5	Transition too long
Data 6	Not used (was unresolved transition)
Data 7	Not used (not used on SWIM)

$2 Write CRC A write here sets the CRC bit in the FIFO, causing the CRC to be written after the last bit of data.

$3 Parameter Data A two bit counter addresses parameter RAM from this location. The counter is reset by a write to the Write Zeroes location ($6). These set up the bit cell timings and the pre-comp values in write mode. (note in the ISM the counter was four bits, the last four values of which are the same as here. The SWIM2 can be thought of as identical to the ISM where the two high order addresses of the four bit counter are don't cares)

Address	Data	
00	Late/xxxx	(first nibble only)
01	*Time0*	(defines step increment, hardwired) (set to 1uS in MFM, 2uS in GCR) (based on 16M clock)
10	Early/xxxx	(first nibble only)
11	*Time1*	(not used)



Late/xxxx and Early/xxxx store two nibbles where the xxxx nibble is ignored. This data is used to append the cell count time determined by time0 as a function of data pattern to achieve the pre-compensation function. The nominal value is $7. Each count will increase or decrease the cell time by one clock period.

$4 Phase Register The phase lines can be programmed as either inputs or outputs. Data bits 0-3 represent phase lines 0-3. Data bits 4-7 act as data direction control for the phase lines 0-3. For example a one in data bit 4 means phase 0 is set as an output, a zero would mean it was an input. Phase 0 would then be written or read in bit 0. On reset all phase lines are set to output a zero.

When in test mode a read of the phase register will return the value of the bytes of zeroes counter, not the phase register.

$5 Setup Register This register sets the various modes of operation. It is reset to all zeroes except as noted.

Data bit 0	*=0 don't invert wrdata (neg pulses)* *=1 invert wrdata (pos pulses)* (was able to select Q3 as output)
Data bit 1	sets 3.5 general purpose output
Data bit 2	= 0 MFM mode; =1 GCR mode.
Data bit 3	= 0 normal; =1 clock divided by two. Note the clock to SWIM2 may be different than SWIM. If supplied a 16M clock SWIM2 will read and write 2,3,4 us MFM cells and 2,4,6 us GCR cells with this bit set to zero. With a 32M clock input SWIM2 will read and write 1,1.5,2 us MFM cells, and should have this bit set to one to generate 2,3,4 us MFM cells and 2,4,6 us GCR cells.
Data bit 4	*Test mode. (note: does not require bit 2 to be set to be in test mode).* *Causes bytes of zeroes count to appear on phase register.*
Data bit 5	0 = Apple data mode; 1 = IBM mode.
Data bit 6	=0 MFM writes; =1 GCR data writes.
Data bit 7	=0 *(was motor timeout)*

$7 Handshake Register Read only

Data bit 0	Mark	Next byte in FIFO = Mark
Data bit 1	CRC zero	CRC was zero, valid when 2nd CRC byte is about to be read from FIFO.
Data bit 2	RDData	Direct read of drive data
Data bit 3	Sense	Direct read of sense input
Data bit 4	=0	*was motor still on*
Data bit 5	Error	A bit in the Error register is set.
Data bit 6	Dat2bytes	FIFO empty in write or full in read when = 1.
Data bit 7	Dat1byte	FIFO has at least one byte in it. *This signal is gated with error in write mode so that if a write error occurs the SWIM will appear empty so to not cause the software to hang.*

$6 &$7 Mode Register Write only

Zeroes @ $6, ones @ $7
The Mode register is controlled bit by bit by writing to either the write zeros or write ones location with the bits that are being modified set to one. To make bit 0 a zero write 00000001 to location $6, to make it a one write 00000001 to location $7. Reset sets all bits to zero.

Data bit 0	Clear FIFO.	A one clears the FIFO. This should be done on successive operations. Read or write mode must be set first.
Data bit 1	Enable1	1 = enable drive 1
Data bit 2	Enable2	1 = enable drive 2
Data bit 3	Action	1 = Action set

Action starts read or write operations. It should be the last thing set. When writing the FIFO should be full before setting. It is cleared by an error on write only.

Data bit 4	Write	1 = write mode; 0 = read.
Data bit 5	Side select	1 = side 1; 0 = side 0
Data bit 6	always 1	(future expansion)
Data bit 7	Motoron	0 = motor disabled; *This runs the output port only, most motor control is through the drive internal register.*

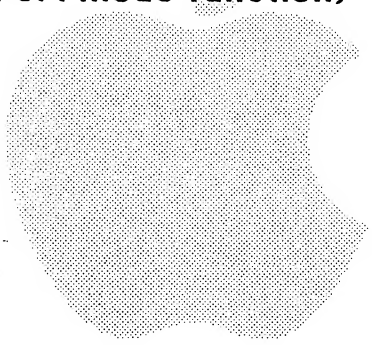
<u>$6 Read status register</u> Read only

Reads contents of mode register.

Special bits

SWIM2 will not support the three new bits defined in SWIM by writes to $02 with action set low since they are all IWM functions. These are Data7 to Override, Data6 to M16/8, Data5 to Modify. These bits have the following definition in SWIM2.

Override	No function in SWIM2 (was an IWM timer function)
M16/8	No finction in SWIM2 (was an IWM timer function)
Modify	No function in SWIM2 (was an IWM Port mode function)



About Half Clocking

The SWIM chip supported both reading and writing data on both edges of the clock. This was done to achieve the highest possible resolution in bit timings and was appropriate considering the general purpose nature of the design. This feature greatly complicates the logic design and test vectors. The SWIM2 is being designed for specific applications where it would be desirable to clock off of only the rising clock edge if at all possible. The following argument shows why I believe this is possible.

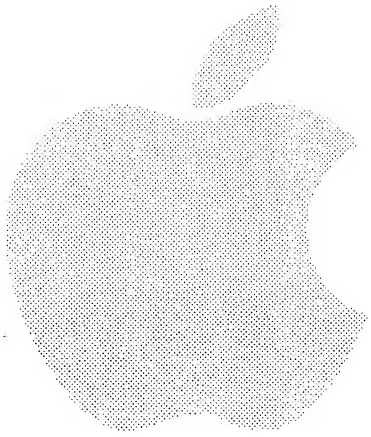
All modern Macs have at least 15.667 MHz clocks available giving clock resolution of 62ns. There are three data formats that must be supported, GCR 2,4,6 uS, MFM 2,3,4 us, and MFM 1,1.5,2 uS. Since the GCR format has its origin in Apple machines its bits cell times are not exactly 2,4,or 6 uS but times which can be perfectly derived from 15.667MHz. This leaves the bit cell times of MFM to consider. The following table shows the number of 15.667MHz clocks in the MFM cell times:

Cell	# clocks	ideal # clocks
1	15.5	15.67
1.5	23.5	23.50
2	31.5	31.33
3	47	47.00
4	62.5	62.67

The table would imply that half clocking is required on four of the five cell times. As stated before in order to support 2.8M MFM SWIM2 would require a 32 MHz clock input. This gives the correct timing for the 1 , 1.5 and 2uS cells. This leaves the problem of correctly writing the 2 and 4uS cell using a 16 MHz clock. If we were to extend the 4 uS cell to be 63 clocks long it would be .5% too long. Likewise, shortening the 2uS cell to 31 clocks would cause it to be 1% too short. Since the format has 5% tolerance a .5% increase in the 4uS cell would not cause any overlap problems. The 4uS cell is the longest cell of the code so stretching it should not cause data recovery problems, as neither would shortening the 2uS cell, it being the shortest cell of the code.

About compatibility

In any redesign of this type the issue of compatibility is of prime importance. SWIM2 will require a new disk driver for the Mac ROM to be functional. 800K GCR mode, although completely different than the current IWM, is the same as the method used by Zone 5 using the PIC with SWIM. 1.44M MFM should appear the same as the current SWIM. 2.88M MFM is a completely new format so there are no backward compatibility issues.



Summary of changes

The table below summarizes the features of the SWIM and the SWIM2.

SWIM	SWIM2
IWM for GCR	No IWM
Programmable windows in MFM or GCR	2 Software selectable sets in MFM, fixed in GCR
Write pre-comp	Write pre-comp
Half clocking	No half clocking
16 MHz clock max.	32 MHz clock max.
Error correction	Fixed windows at any given format
Post compensation	No post compensation
Drive PLL optional	Drive PLL is required
No output sense change	*Output sense programable*

Technical Specification

Write cell times***

1uS		0.989**	uS
1.5uS		1.499**	uS
2uS	1.979*	2.010**	uS
3uS		2.999	uS
4uS	3.989**	4.021*	uS
6uS		5.999	uS

* Written with 15.667 MHz clock
** Written with 31.334 MHz clock
***Write times can be added to or subtracted from by setting the write pre-comp register in one clock resolution.

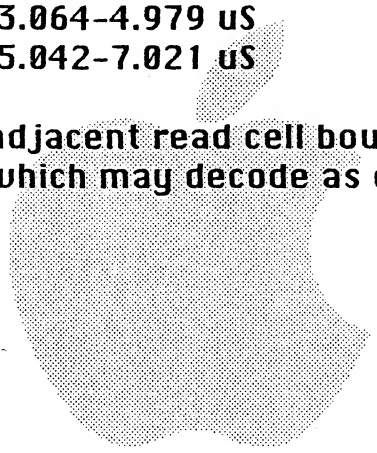
Write pulse width

The write pulse in MFM mode shall be five clock periods long.

Read cell times

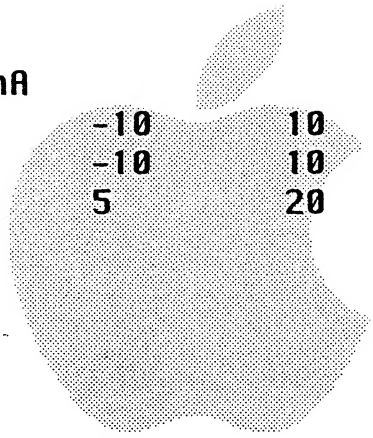
	16MHz	32MHz
1uS		.734-1.245 uS
1.5uS		1.277-1.723 us
2uS		1.755-2.266 us
2uS	1.468-2.489 uS	
3uS	2.553-3.447 uS	
4uS	3.510-4.532 uS	
2uS	0.957-2.999 uS	
4uS	3.064-4.979 uS	
6uS	5.042-7.021 uS	

Note: Gaps between adjacent read cell boundries represent areas of uncertainty which may decode as either possible cell.



DC Specification @ Udd = 4.75 to 5.25U Temp = 0 to 70C

Parameter	Min	Max	Unit
Supply current		50	mA
Input low level		0.8	U
Input high level	2.0		U
Output high level @ I=3.2 mA	2.4		U
Output low level @ I=3.2 mA except the following: Wrreq/ I=10 mA Phase1 I=10 mA Enable1/ or 2/ I=5 mA		0.4	U
Input leakage	-10	10	uA
Output leakage	-10	10	uA
Pullup R Rddata, Sense	5	20	KΩ

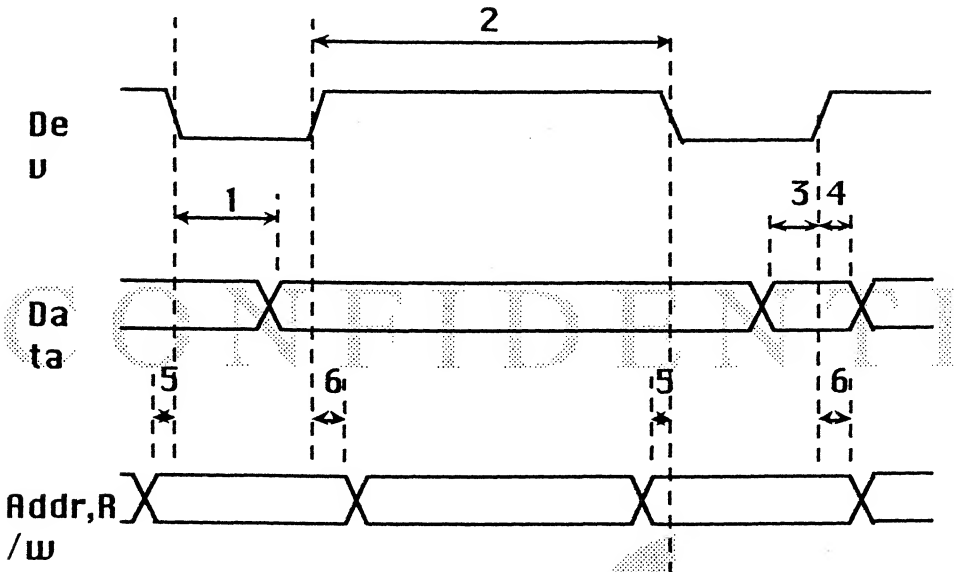


AC Specification

Parameter	Min	Max	Unit
Clockin	0	32	MHz
Duty Cycle	40	60	%
Rise and fall	0	10	nS
Dev/*			
R/W low to Dev/ low	15		nS
Dev/ high to R/W high	0		nS
Add setup to Dev/ low	15		nS
Add hold from Dev/ high	0		nS
Data setup to Dev/ low	35		nS
Data hold from Dev/ high	0		nS
Dev/ rise to data invalid	0		nS

*Dev/ in this case is the logical OR of Q3 and Dev/.

Clock rise to output (Wrdata,Wrreq/,Dat1byte)	0	25	nS
Dev/ rise to output (Phase,Hedsel,Enabl1/ 2/, Motoen/,3.5Sel/)	0	tbd	nS
Async in to Dev/ fall setup	0	tbd	nS



Timing:

1. Dev low to data valid read. 95ns
2. Dev high to dev low. 8 clks
3. Data setup write 35ns
4. Data hold write 0 ns
5. Addr,R/w to Dev low 15ns
6. Addr,R/w hold 0 ns

Pin Description

D0-D7	The bi-directional CPU data bus
A0-A2	Address inputs for register select
R/W	Bus read write control input
Dev/	Device select input
Q3	OR'ed with Dev/ (input)
Reset/	Hardware reset input
Wrdata	Write data output to disk
Wrreq/	Write enable output to disk
Motoen/	Motor on indication output
Enabl1/	Drive enable output to disk
Enabl2/	Drive enable output to disk
Sense	Readable input used to read write protect status
Rddata	Data input from drive
Clockin	Input clock to SWIM2
Phase0-3	Bi-directional controls from disk
Hedsel	Head select output to disk
Dat1byte	Output indicating FIFO contains data
3.5sel	General purpose output

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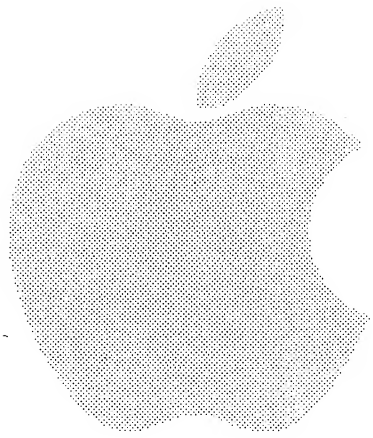

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